IBIS Open Forum Minutes

Meeting Date: **May 25, 2018**
Meeting Location: **SPI-E IBIS Summit, Brest, France**

VOTING MEMBERS AND 2018 PARTICIPANTS

ANSYS	Curtis Clark
Applied Simulation Technology	(Fred Balistreri)
Broadcom	(Yunong Gan)
Cadence Design Systems	Brad Brim, Ken Willis, Ambrish Varma
Cisco Systems	Stephen Scearce, Cassie Yan, Baosh Xu
CST	Stefan Paret
Ericsson	Anders Ekholm, Zilwan Mahmod, Guohua Wang
GLOBALFOUNDRIES	Steve Parker
Huawei Technologies	(Hang (Paul) Yan)
IBM	Greg Edlund, Luis Armenta, Hubert Harrer*
Infineon Technologies AG	(Christian Sporrer)
Intel Corporation	Hsinho Wu, Michael Mirmak, Nilesh Dattani Fernando Mendoza Hernandez, Varun Gupta Subas Bastola, Hansel Dsilva, Gianni Signorini*
IO Methodology	Lance Wang
Keysight Technologies	Radek Biernacki, Ming Yan, Heidi Barnes Pegah Alavi
Maxim Integrated	Joe Engert, Yan Liang
Mentor, A Siemens Business	Arpad Muranyi, Weston Beal, Raj Raghuram Carlo Bleu, Mikael Stahlberg, Yasushi Kondou Vladimir Dmitriev-Zdorov, Nitin Bhagwath*
Micron Technology	Randy Wolff, Justin Butterfield
NXP	(John Burnett)
Qualcomm	Kevin Roselle, Tim Michalka
Raytheon	Joseph Aday
SiSoft	Mike LaBonte*, Walter Katz, Todd Westerhoff
Synopsys	Ted Mido, Adrien Auge, Scott Wedge
Teraspeed Labs	Bob Ross
Xilinx	Ravindra Gali
ZTE Corporation	(Shunlin Zhu)
Zuken	Michael Schaeder*, Takayuki Shiratori

OTHER PARTICIPANTS IN 2018

Google	Zhiping Yang
Haskware	David Banas

John Baprawski, Inc.	John Baprawski
KEI Systems	Shinichi Maeda
Lattice Semiconductor	Dinh Tran, Maryam Shahbazi
OmniVision	Sirius Tsang
Politecnico di Milano	Flavia Grassi*, Xinglong Wu*
Politecnico di Torino	Tommaso Bradde*, Marco De Stefano*, Paulo Manfredi* Riccardo Trinchero*, Stefano Grivet-Talocia*
Ricoh	Kazuki Murata
RITA Electronics Ltd.	Kenichi Higashiura, Hiroyuki Motoki
SAE-ITC	(Jose Godoy)
Signal Metrics	Ron Olisar
Socionext	Megumi Ono
SPISim	Wei-hsing Huang
Stanford University	Tom Lee
STMicroelectronics	Aurora Sanna*, Olivier Bayet*
Toshiba	Yasuki Torigoshi, Yoshinori Fukuba
Université de Bretagne Occidentale	Mihai Telescu*, Charles Canaff*
University of Illinois	José Schutt-Aine*
University of Siegen	Elmar Griese*
University of Technology Hamburg	Torben Wendt*

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date	Meeting Number	Meeting Password
June 8, 2018	624 227 121	IBISfriday11

For teleconference dial-in information, use the password at the following website:

http://tinyurl.com/y7yt7buz

All teleconference meetings are 8:00 a.m. to 9:55 a.m. US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting.

NOTE: "AR" = Action Required.

OFFICIAL OPENING

The IBIS Open Forum Summit was held in Brest, France at Le Quartz following the 2018 SPI conference. About 19 people representing 12 organizations were recorded in attendance.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

http://www.ibis.org/summits/may18/

Mike LaBonte opened the summit, thanking SPI conference chair Mihai Telescu for his assistance in making arrangements for the summit. Mike noted that the use of IBIS models is quite prevalent, involved in the design of most electronics with chip to chip digital signaling. The IBIS Model Library web page listed a large number of sources from which IBIS models were available. Mike thanked the summit sponsors Mentor, a Siemens Business, SiSoft, Teraspeed Labs, and Zuken. He said that although there would be no voting, minutes of the summit would be posted as an official IBIS meeting.

IBIS UPDATE
Mike LaBonte, SiSoft, USA

Mike LaBonte gave a brief overview of the IBIS Open Forum organization and its activities. The Open Forum was near the final stages of completing the IBIS 7.0 specification, which Mike predicted might be ratified in November of 2018. He noted that while IBIS held summit meetings 5 or 6 times each year and held Open Forum teleconferences every 3 weeks, much of the detailed work of completing change documents (BIRDs) was done in weekly meetings, usually three per week, sometimes four. Mike described one of the key new features in IBIS 7.0, interconnect modeling using IBIS-ISS and Touchstone.

IBIS-COMPATIBLE MACROMODEL AND INTERCONNECT SIMULATION TECHNIQUES
José Schutt-Aine, University of Illinois, USA

With the stated objective of including non-linear effects in the time domain simulation of systems, José described possible process flows for using transmission lines, white-box macro models, black-box macro models, and IBIS models in the same simulation. While lossless transmission lines are easily modeled directly, lossy transmission lines that are frequency-dependent and linear could be converted to white-box macro models, which could then go through model order reduction and be stamped into the simulation matrix as poles and zeros. Advanced I/O buffer models could be implemented as black-box macro models for intellectual property protection. From those impulse responses could be derived, and then equivalent SPICE subcircuits could be synthesized. Machine learning could be used for I/O buffer models, resulting in X-parameters, which are able to handle non-linear devices.

A question was asked about existing examples of using X-parameters in simulation. José said that Keysight, for example, had that in place.

ON AUTOMATED GENERATION OF BEHAVIORAL PARAMETERIZED MACROMODELS PART I: ALGORITHMIC ASPECTS
Tomasso Bradde, Stefano Grivet-Talocia, Marco De Stefano, Alessandro Zanco, Politecnico di Torino, Italy
[Presented by Tomasso Bradde, Politecnico di Torino, Italy]

Tommaso said the main objective was fast simulation with non-linear elements, by describing behavior with respect to parameter variations. This would start with separate S-parameter files for different parameter values. Then, a model structure to fit the data to would be formed. Non-linearity may cause fitting problems. Parameterized Sanathanan-Koerner was used to find the known equation elements. The resulting computation requirement of that was cubic. The results were good but much time and memory were required. To improve performance, least squares methods were used to decouple the responses and find the denominators. This allowed the decoupled responses to be solved individually, using less resources. The accuracy of that approach was not as good for attenuated responses, however. A method of weighting the responses to normalize their scales could be used to move them into a better range, improving accuracy.

A question was asked about possible formats for storing the models and data. Tommaso said that SPICE tools support a number of formats for this, including SPICE circuits.

ON AUTOMATED GENERATION FO BEHAVIORAL PARAMETERIZED MACROMODELS PART II: SPICE EQUIVALENTS AND APPLICATIONS
Marco De Stefano, Stefano Grivet-Talocia, Tomasso Bradde, Alessandro Zanco, Politecnico di Torino, Italy
[Presented by Marco De Stefano, Politecnico di Torino, Italy]

Marco said that SPICE circuits directly extracted from complex electronic systems were not only slow to simulate, they would sometimes be unstable, resulting in run away or erroneous voltages. SPICE circuits generated from macro model equations might offer better performance. The denominator of the model equation allowed for poles with a trajectory such that there was a positive real component above a certain frequency, resulting in the instability.

Marco presented a theorem in three parts that could be used to help guarantee model stability. Adaptive sampling would be used to enforce constraints on linear inequality using a parameterized Sanathanan-Koerner approach. A fast method to do that was shown. In a test, accuracy was nearly as good as before adaptive sampling, and the model was stable. To further ensure stability, perturbation of the denominator coefficients was used to look for conditions that would lead to local minima, in a process that optimized the numerator coefficients. Marco noted that the control parameter inputs to the circuits could be implemented as global variables, subcircuit parameters, or with extra input pins. The choice would depend on whether it needed to be dynamic. Marco showed a number of simulation examples, concluding that after 25 test cases, maximum error was less than 1% and performance was 10 to 100 times better than directly extracted SPICE.

IBIS-AMI AND JITTER
Mike LaBonte, SiSoft, USA

Mike began with a description of what different types of jitter and noise looked like. He gave an overview of the IBIS-AMI jitter and noise parameters in IBIS 5.0, IBIS 6.1, and those to be included in IBIS 7.0. Mike showed the process flows for using jitter and noise parameters in the cases where the Rx has AMI_GetWave() and does return clock times, where it exists but does not return clock times, and in statistical analysis. In each case the EDA tool provided much of the jitter and noise processing. Mike showed examples of IBIS-AMI simulation outputs with

Gaussian, deterministic, and sinusoidal jitter, as well as voltage domain noise. After all jitter and noise had been applied, they were used by the EDA tool to recover the digital data stream from the output waveform and clock times, using Rx_Receiver_Sensitivity to model inherent hysteresis.

DDR5 EQUALIZATION OPTIONS WITH IBIS

Arpad Muranyi, Nitin Bhagwath, Mentor, a Siemens Business, USA
[Presented by Nitin Bhagwath, Mentor, A Siemens Business, USA]

Nitin gave an overview of the types of equalization used by DDR5 devices. He said that IBIS-AMI is not the only solution for modeling DDR5 equalization, noting that IBIS-AMI is designed to support the calculation of a bit error rate (BER), whereas DDR5 does not have a BER requirement. Also, IBIS-AMI was designed for the case where clocks were recovered from received waveforms, whereas DDR5 used separate clock signals. Furthermore, the SerDes links modeled by IBIS-AMI were point to point, whereas DDR5 topologies were multi-drop. Nitin said that since equalization was being used for single-ended signals in DDR5 and IBIS-AMI was designed for differential signals, special measures would be required to support non-linear effects such as voltage bias changes. Therefore, IBIS-AMI has no easy way to incorporate the ground bounce effects of simultaneously switching outputs (SSO).

Nitin listed means other than IBIS-AMI to simulate DDR5 signals, indicating that Verilog-A might find the best support. He showed example DDR5 topologies and portions of Verilog-A models for them. While a system implemented in Verilog-A could have similarities to IBIS-AMI, it would be able to modify the analog model at each time step to incorporate non-linear effects. He showed results from such a simulator. When non-ideal power and ground supplies were inserted, the comparison between the Verilog-A simulator and IBIS-AMI showed significant differences, with the more accurate Verilog-A simulation showing a more closed inner eye. Nitin said it took 70 seconds to simulate 4096 bits. That was not as fast as IBIS-AMI, but much faster than SPICE. Because BER is not calculated, shorter simulations might work well for DDR5.

A question was asked about why the non-ideal power and ground simulation showed an outer eye that was reduced along with the inner eye. Nitin said the very simple power and ground models used lead to that. Mihai Telescu noted that the limitations of IBIS-AMI were intrinsic, asking why existing technologies had not been used. Nitin said that technical issues are not always the primary difficulty, and that if a solution is not plug-and-play there will be forces against adoption unless major vendors support it.

IBIS [MODEL SELECTOR] IMPROVEMENT PROPOSAL

Michael Schaeder*, Bob Ross**, *Zuken, Germany; **Teraspeed Labs, USA
[Presented by Michael Schaeder, Zuken, Germany]

Michael showed examples of file sizes for some of the larger available IBIS files, noting that the larger files can be somewhat slow to edit. He suggested that unnecessary content could be removed from some files to make them smaller, showing an example where 192 models were present in [Model Selector] keywords. Michael said that EDA software can help by allowing users to choose the models to be used in any given simulation, rather than editing the IBIS files to place the desired model in the first line. However, setting the preferred model name for each [Model Selector] could be tedious.

He showed a proposed [Model Group Selector] keyword, which had an additional model_group column. Each model group name would be present across all selectors, allowing the selection of one group name to control the choice of model for each [Model Group Selector]. This would allow users to select the common combinations of models by making only a single choice, not one for each [Model Selector]. Michael proposed that a BIRD would be written to add [Model Group Selector] to IBIS. He also suggested other simple steps that could be taken by model makers and EDA vendors to make [Model Selector] easier to use.

A question was asked about the possibility that two lines in a [Model Group Selector] would have the same group name. Michael said that would not be allowed. Another question was why IBIS files could be so large. Nitin Bhagwath said that there were some "technology IBIS files" containing a [Model] for each known I/O buffer technology, and there could be many of those. It was noted that early FPGA design software produced such "unpruned" IBIS files, and that another solution could be to split up models into separate IBIS files, where there are groups of models that would never be used together.

CONCLUDING ITEMS

In closing, Mike LaBonte thanked the attendees, the presenters, and the sponsors. He also thanked SPI Chair Mihai Telescu for once again inviting IBIS to SPI, and for his assistance and hospitality. Mike ended the meeting, noting that Mihai Telescu was prepared to conduct a walking tour of Brest, which a number of attendees enjoyed.

NEXT MEETING

The next IBIS Open Forum teleconference meeting will be held on June 8, 2018. The following IBIS Open Forum teleconference meeting is tentatively scheduled on June 29, 2018. Votes on BIRD189.6 and BIRD194 are scheduled for this meeting.

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NOTES

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This meeting was conducted in accordance with ANSI guidance.

All inquiries may be sent to info@ibis.org. Examples of inquiries are:

- To obtain general information about IBIS.
- To ask specific questions for individual response.
- To subscribe to the official ibis@freelists.org and/or ibis-users@freelists.org email lists (formerly ibis@eda.org and ibis-users@eda.org).
- To subscribe to one of the task group email lists: ibis-macro@freelists.org, ibis-interconn@freelists.org, or ibis-quality@freelists.org.
- To inquire about joining the IBIS Open Forum as a voting Member.
- To purchase a license for the IBIS parser source code.
- To report bugs or request enhancements to the free software tools: ibischk6, tschk2, icmchk1, s2ibis, s2ibis2 and s2iplt.

The BUG Report Form for ibischk resides along with reported BUGs at:

http://www.ibis.org/bugs/ibischk/
http://www.ibis.org/ bugs/ibischk/bugform.txt

The BUG Report Form for tschk2 resides along with reported BUGs at:

http://www.ibis.org/bugs/tschk/
http://www.ibis.org/bugs/tschk/bugform.txt

The BUG Report Form for icmchk resides along with reported BUGs at:

http://www.ibis.org/bugs/icmchk/
http://www.ibis.org/bugs/icmchk/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.ibis.org/bugs/s2ibis/bugs2i.txt
http://www.ibis.org/bugs/s2ibis2/bugs2i2.txt
http://www.ibis.org/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

http://www.ibis.org/

Check the IBIS file directory on ibis.org for more information on previous discussions and results:

http://www.ibis.org/directory.html

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SAE STANDARDS BALLOT VOTING STATUS

Organization	Interest Category	Standards Ballot Voting Status	April 13, 2018	May 4, 2018	May 18, 2018	May 25, 2018
ANSYS	User	Active	X	-	X	-
Applied Simulation Technology	User	Inactive	-	-	-	-
Broadcom Ltd.	Producer	Inactive	-	-	-	-
Cadence Design Systems	User	Active	X	X	X	-
Cisco Systems	User	Inactive	-	-	-	-
CST	User	Inactive	-	-	-	-
Ericsson	Producer	Inactive	-	-	-	-
GLOBALFOUNDRIES	Producer	Active	X	X	X	-
Huawei Technologies	Producer	Inactive	-	-	-	-
IBM	Producer	Active	-	-	X	X
Infineon Technologies AG	Producer	Inactive	-	-	-	-
Intel Corp.	Producer	Active	X	X	X	X
IO Methodology	User	Active	X	X	X	-
Keysight Technologies	User	Active	X	X	X	-
Maxim Integrated	Producer	Inactive	-	-	-	-
Mentor, A Siemens Business	User	Active	X	X	X	X
Micron Technology	Producer	Active	X	X	X	-
NXP	Producer	Inactive	-	-	-	-
Qualcomm	Producer	Inactive	-	-	-	-
Raytheon	User	Inactive	-	-	-	-
SiSoft	User	Active	X	X	X	X
Synopsys	User	Active	-	X	X	-
Teraspeed Labs	General Interest	Active	X	X	X	-
Xilinx	Producer	Inactive	-	-	-	-
ZTE Corp.	User	Inactive	-	-	-	-
Zuken	User	Inactive	-	-	-	X

Criteria for SAE member in good standing:

- Must attend two consecutive meetings to establish voting membership
- Membership dues current
- Must not miss two consecutive meetings

Interest categories associated with SAE standards ballot voting are:

- Users - members that utilize electronic equipment to provide services to an end user.
- Producers - members that supply electronic equipment.
- General Interest - members are neither producers nor users. This category includes, but is not limited to, government, regulatory agencies (state and federal), researchers, other organizations and associations, and/or consumers.